

REMARKS/ARGUMENTS

The Applicant appreciates the Examiner's continued consideration. In the present Office Action, the Examiner has objected to the drawings, rejected Claim 9 under 35 U.S.C. § 112, and Claims 1-3, 6-9, and 13-20 were rejected under 35 U.S.C. § 103(a). The Applicant addresses each of these rejections below. The Applicant is appreciative of the Examiner's continued indication of allowance for Claims 4-5 and 10-12.

Objection to the Drawings

The Examiner objected to the figures based on the Examiner's contention that the specification did not disclose an inverter in FIGURE 2 for inverting a MSB result prior to entering an OR.

The Applicant has amended Figure 2 such that it is in its original form as filed and is hereby included as Attachment A. The inverter added with the Response dated 8/8/05 has been removed. At the same time, Applicant has also added a new drawing sheet, FIGURE 6, as Attachment B. New FIGURE 6 is the embodiment disclosed in replacement FIGURE 2 with the addition of an inverter 70 before the OR gate 38. Support for the new figure is found in original claim 9 and within the specification at page 11 lines 19-21. The text of the specification and the brief description has been amended to reflect the new FIGURE 6. No new matter has been added.

Rejection based upon 35 U.S.C. § 112, first paragraph

The Examiner indicated that the Claim 9 was rejected based upon 35 U.S.C. § 112, first paragraph for failure to comply with the written description requirement and comply with the enablement requirement. The Applicant traverses this rejection.

Applicant has added new FIGURE 6. In conjunction with exemplary support for the limitations of Claim 9 at page 11, lines 19-21, the specification provides an enabling written description for one skilled in the pertinent art.

Applicant respectfully requests reconsideration of the rejection and believes Claim 9 to be enabled and in compliance with the written description requirement of 35 U.S.C. § 112, first paragraph.

Rejection based upon 35 U.S.C. § 103(a) (Bonnet et al. in view of Jain et al.)

The Examiner rejected Claims 1-3, 6-9, 13-17 and 19-20 under 35 U.S.C. § 103(a) as being obvious over Bonnet et al. ("Bonnet et al.") (USP 6,321,248) in view of Jain et al. ("Jain et al.") (USP 6,061,781). Respectfully, the Applicant traverses the rejection and requests withdrawal.

Allowability of Claims 1-3

Regarding Claims 1-3, the Examiner has not overcome the burden of providing a *prima facie* case of obviousness as required by MPEP § 2142. Specifically, all the claim limitations are neither taught nor suggested in the prior art references. As an example, Bonnet et al. does not teach "determining an overflow output based upon the first and second fixed-point format and predicting whether an arithmetic operation of the first operand with the second operand will yield a result that exceeds the overflow output."

Therefore, the Examiner has not shown that the prior art cited teaches or suggests all the claim limitations of Claim 1. Applicant respectfully requests reconsideration of the rejection and believes Claim 1 to be allowable.

Regarding Claim 2, all the limitations of Claim 2 are not taught by the references cited. Furthermore, Applicant traverses the Examiner's assertion that Claim 2 has the same limitations as Claim 1. Specifically, the Examiner has failed to show that Bonnet et al. teach the limitation of multiplication. Though Bonnet et al. may disclose a type of overflow circuit for some arithmetic operation (i.e. addition), it does not disclose multiplication. Multiplication is not mentioned in the cited prior art nor is it taught for purposes of overflow detection. Regarding overflow detection, cases involving addition or subtraction often require a different rule or logic than multiplication, a significantly different arithmetic operation. Applicant respectfully requests reconsideration of the rejection and believes Claim 2 to be allowable.

Regarding Claim 3, the Applicant traverses the Examiner's assertion that Claim 3 has the same limitations as Claim 2. Applicant points out that not only is the preamble of Claim 2 distinct from Claim 3, so is the recitation of virtually every limitation of the respective Claims. Claim 2 is distinct from Claim 3 and cannot be rejected on the same basis without identifying a limitation-by-limitation basis for an obviousness rejection. Furthermore, Bonnet et al. does not disclose all the limitations of Claim 3. By example, Bonnet et al. does

not teach or suggest any method for clamping, or even a method for clamping fixed-point multipliers having a step for determining a clamping value based on the first fixed-point format of the first operand and the second fixed-point format of the second operand. For the at least the above reasons, Applicant contends that the Examiner has failed to overcome the burden of setting forth a *prima facie* case of obviousness. Applicant respectfully requests reconsideration of the rejection and believes Claim 3 to be allowable.

Allowability of Claims 6-9

Regarding Claim 6, the Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations as required by MPEP § 2142. By example, the Examiner has failed to show that Bonnet et al. teach or suggest a method of processing multiplier data paths. Bonnet et al. does not once specifically mention multiplication. Claim 6 requires a “plurality of operands, each having a fixed-point format.” As taught by the Applicant on page 5 of the Application as filed, a representative “addition and subtraction” and “multiplication” rules for using fixed-point format. Bonnet et al. does not teach nor suggest all the limitations of amended Claim 6. Regardless to the above arguments, the Applicant has amended Claim 6 to further clarify the method claimed by adding the step of “selecting a rule for a multiplication operation”, which is not disclosed in the cited prior art. Applicant respectfully requests reconsideration of the rejection and believes Claim 6 to be allowable.

Regarding Claim 7, the Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations as required by MPEP § 2142. By example, the Examiner refers the Applicant from col. 3 to col. 4 and contends that Bonnet et al. teach “multiplying the first and second operands to generate a result not to exceed a predetermined number of bits.” Applicant traverses this contention, as Bonnet et al. does not teach nor suggest this claim limitation. In fact, Bonnet et al. does not even mention multiplication.

Furthermore, the Examiner has failed to show that Bonnet et al. teach or suggest the step of “determining an initial clamping predictor bit based upon the first operand and the second operand.” The Examiner has failed to distinctly point to where Bonnet et al. teach or suggest this claim limitation. The references cited do not perform a clamping function as contemplated by the Applicant and do not teach the above cited claim limitation. Even further, the Examiner has failed to show that Bonnet et al. teach or suggest the step of “logically ORing the initial clamping predictor bit and a most significant bit of the result to

produce a final clamping predictor bit.” The Examiner refers the Applicant to col. 2 lines 1-12, but the Applicant fails to see how this section of Bonnet et al. discloses the identified limitation of Claim 7. Applicant respectfully requests reconsideration of the rejection and believes Claim 7 to be allowable.

Regarding Claim 9, the Applicant has amended FIGURE 2, added FIGURE 6, and amended the specification. The identified amendments, the new figure, original Claim 9 and the specification support the limitation disregarded by the Examiner. The Examiner previously indicated that Claim 9 would be allowable if placed in independent form. The Applicant contends that independent Claim 9 is in condition for allowance and respectfully requests reconsideration of the rejection.

Allowability of Claims 13-20

Regarding amended Claim 13, the Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations as required by MPEP § 2142. Bonnet et al. neither teach nor disclose the multiplication overflow detection circuit of amended Claim 13. By example, Bonnet et al. does not teach an overflow detection circuit wherein determining the initial clamping predictor bit includes determining a number of logical ones in each of the operands and summing the number of logical ones to determine whether the sum exceeds a pre-determined number. Applicant contends that independent Claim 13 is in condition for allowance and respectfully requests reconsideration of the rejection.

Regarding Claim 15, the Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations as required by MPEP § 2142. The Examiner has not distinctly pointed out all of the elements of the claim as being disclosed or suggested by the cited references.

The Applicant respectfully traverses the Examiner's contention that Claim 15 is a circuit claim of Claim 7. Claim 15 includes a clamp bit register and a result register not found in Claim 7. Furthermore, Claim 15 does not require logical ORing. Neither Bonnet et al. nor Jain et al. teach or suggest the circuit of Claim 15, which includes a clamp bit register, a result register, and logical ORing. Favorable reconsideration of Claim 15 is requested.

Regarding Claim 16, the Examiner has not provided a *prima facie* case of obviousness required by MPEP § 2142. By example, Claim 16 includes a clamp bit register and a result register. The Applicant traverses the rejection as the Examiner has not shown that the

references teach or suggest all the claim limitations. The Applicant furthermore traverses the Examiners contention that Claim 15 and Claim 16 have the same limitations. By example, Claim 16 has further limitations that include, but not limited to, “wherein the multiplexer selects one of the clamp value register input and the result register input based upon a logical level of the clamp bit register in order to make the selected input the output of the multiplexer. Favorable, reconsideration of Claim 16 is requested.

Regarding amended Claim 17, the Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations as required by MPEP § 2142. By example, the Examiner has failed to show that Bonnet et al. teach or suggest an overflow detection circuit as claimed in amended Claim 17.

Furthermore, the Examiner has failed to show that Bonnet et al. teach or suggest where the “the clamp bit input is logically ORed with a most significant bit of the result stored in the result register.” The Examiner refers the Applicant to col. 2 lines 1-12, but the Applicant fails to see how this section of Bonnet et al. discloses the identified limitation of Claim 17. Bonnet et al. furthermore does not teach other logic that processes the multiplexor output for pipelining. Favorable reconsideration of Claim 17 is requested.

Misapplied VALSAT Limitation of *Bonnet et al.*

The Examiner has also not provided a *prima facie* case of obviousness as the Examiner has pointed to a single element in the Bonnet et al. reference to represent three completely distinct elements having distinct functions. Specifically, the Examiner has identified the clamp bit register (See 1/25/06 OA page 9), the clamping value (See 1/25/06 OA page 5) and overflow outputs (See 1/25/06 OA page 4) to be equivalent to the VALSAT* and VALSAT as disclosed in Bonnet et al.. The Examiner’s assertions are not easily followed by the Applicant and are apparently inconsistent. The Applicant contends that VALSAT* and VALSAT as disclosed in Bonnet et al. can not be equivalent to the clamp bit register, the clamping value and the overflow outputs. Applicant does not see how the VALSAT* and VALSAT as disclosed in Bonnet et al. is equivalent to three separate and distinct claim elements. The Applicant contends that the misapplied VALSAT limitation is an element to Applicant’s contention that the Examiner has not overcome his burden for showing *prima facie* obviousness. Further clarification from the Examiner is requested.

Jain et al. As Improper Reference

The Applicant respectfully submits that the combination of Bonnet et al. and Jain et al. can't be properly maintained, as the references teach away from the Applicant's invention. Jain et al. does not contemplate a clamping function as in the Applicant's invention. Jain et al. fails to enable one skilled in the art to make or practice the invention, as there is no specific structure shown that can perform a "stop execution", and Jain et al. is illogically inconsistent. Though Jain et al. discloses a "stop execution of the integer divide micro instruction" when "overflow is detected" (Col. 16, Ln. 47-65), Jain et al. goes on further to teach that "a flow chart 700 is provided illustrating a method for performing integer division according to the present invention" (Col. 17, Ln. 6-8) and then later discloses that "At block 726, a signal indicating detection of a divide overflow is generated by the microprocessor. Flow then proceeds to block 730" (Col. 17 Ln. 56-60) where the method completes. Jain et al. is inherently inconsistent and can not independently teach both a stop execution and completion upon detection of an overflow as these are not separate embodiments. Applicant respectfully requests reconsideration of the rejection and believes Claims 1-20 are patentably distinct from the cited prior art.

Rejection based upon 35 U.S.C. § 103(a) (Bonnet et al. in view of Jain et al., in further view of Kim)

The Examiner rejected Claim 18 under 35 U.S.C. § 103(a) as being obvious over Bonnet et al. (USP 6,321,248) in view of Jain et al. (USP 6,061,781), in further view of Kim (USP 5,369,438). Respectfully, the Applicant traverses the rejection and requests withdrawal.

The Examiner has failed to provide a *prima facie* case of obviousness. Specifically, the Examiner has failed to show that the cited references teach or suggest all the claimed limitations of amended Claim 18 as required by MPEP § 2142. Furthermore the Applicant contends that the prior art fails to suggest the desirability of the combination of the cited references. Claim 18 has been amended and Applicant contends that it is patentably distinct from Bonnet et al. and Jain et al. as discussed above. Favorable reconsideration of Claim 18 is requested.

The Applicant contends that the amendments and the above remarks, place the application in condition for allowance. Applicant respectfully requests reconsideration.

Applicant has added one independent claim, the \$200 fee for the additional independent claim and any other fees should be charged to Deposit Account 23-2053. Any required petition should be considered provisionally made.

Respectfully submitted,



Jonathan M. Fritz

Registration No. 52,922

Dated: April 25, 2006

P.O. ADDRESS:

WHYTE HIRSCHBOECK DUDEK S.C.

One East Main Street, Suite 300

Madison, WI 53703

Customer No. 56080